REMARKS

Claims 1-12 are presently pending and stand rejected. Reconsideration is requested. Claim 13 is added as new.

Claims 1-12 were rejected under 35 U.S.C. 103(a) as being obvious from the combination of Rana in view of Agarwal. Claims 1 and 9 recite, among other limitations, "the contents of the memory location associated with the address received from the code address bus being incremented responsive to receipt of the address". Claim 5 recites, among other limitations "incrementing a memory location mapped to the address associated with the instruction".

Examiner has indicated that "It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the flagging of the executed code of Rana with the storing of an incremented value associated with executed code of Agarwal."

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)." MPEP 2143.01

In Rana, "The code coverage data is comprised of predetermined bit patterns providing information on the access to the monitored memory, wherein the predetermined bit patterns may be varied for different tests run through the monitored memory." Rana, Abstract (Emphasis Added). For example, Rana, Col. 8, Line 31+ states that "For example, hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." (Emphasis Added).

Modifying Rana with the storing of an incremented value would make Rana inoperable to determine the code coverage of the different individual tests run through the monitored memory. Since the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. Accordingly, Assignee traverses the rejection to claims 1, 5, and 9, and dependent claims 2-4, 6-8, and 10-13.

Claim 2 recites, among other limitations, "an address multiplexer for making a first selection between the input and an address counter, and for providing the first selection to the memory".

Examiner has indicated that Rana discloses "the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, where the cover[age] memory is isolated from the addressing from the monitored memory, thus selecting counter circuit, this is interpreted as an address multiplexer for making a selection between the input and an address counter, and for providing the selection to the memory (See Col. 4, line 65 to Col. 5, line 3 and Col. 5, lines 11-18)."

"Claims must be given their broadest reasonable interpretation." MPEP 2111. However, the broadest reasonable interpretation of "an address multiplexer for making a first selection between the input and an address counter" cannot be interpreted to cover merely "the code coverage memory being concurrently addressed with the monitored memory and the use of a counter circuit of memory location, where the cover[age] memory is isolated from the

addressing from the monitored memory, thus selecting counter circuit", even if the foregoing characterization is correct. It is noted that the foregoing does not teach a "multiplexer". Accordingly, Assignee traverses the rejection to claims 2, as well as claim 10 and requests that Examiner withdraw the rejection.

Claim 3 recites "a data multiplexer for making a second selection between an increment signal and a clear signal, and for providing the second selection to the memory". Examiner has indicated that "Rana teaches the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to '00' and changing it to value 'ff', and Agarwal teach the values for a test run being '1' for set, thus '0' being the cleared value, this is interpreted as a data multiplexer for making a selection between an increment signal and a clear signal, and for providing the selection to the memory (See Col. 8, lines 31-44 and See Agarwal, paragraph 0123)."

Rana, Col. 8, Lines 31+ states that "For example, hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." (Emphasis Added). Assignee submits Rana does not teach that "hexadecimal value '00'" is "changed to value 'ff'" as indicated by Examiner. Rather, "hexadecimal 'ff' may be loaded from the register 58 to the code coverage memory 10 in one test, and hexadecimal '00' may be loaded in another test." Moreover it is also submitted that even if "hexadecimal value '00'" is "changed to value 'ff'", the foregoing does not amount to incrementing. Accordingly, Assignee traverses Examiner's characterization of Rana.

Moreover, the broadest reasonable interpretation of "a data multiplexer for making a selection between an increment signal and a clear signal, and for providing the selection to the memory" cannot be interpreted to cover merely "the code coverage memory storing code coverage data of predetermined bit patterns that includes setting the hexadecimal value to '00' and changing it to value 'ff'", even if the foregoing characterization of Rana is correct. It is noted that the foregoing does not explicitly teach a "multiplexer", or selecting "between an increment signal and a clear signal".

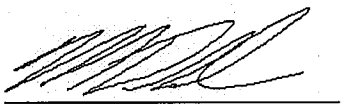
With regards to Agarwal, Examiner has indicated that Agarwal "teach the values for a test run being '1' for set, thus '0' being the cleared value". Assignee respectfully submits that "'1' for set" is entirely different from "an increment signal". Accordingly, Assignee traverses the rejection to claim 3, as well as claim 11, and requests that Examiner withdraw the rejection.

CONCLUSION

For at least the foregoing reasons, Assignee submits that each of the pending claims are now in a condition for allowance. Accordingly, Examiner is requested to pass this case to issuance.

It is believed that all monies for the actions described herein are provided with this correspondence. To the extent that additional monies are required for any of the actions requested in the correspondence, Commissioner is authorized to charge such fees and credit any overpayments to deposit account 13-0017.

Respectfully Submitted



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